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2.	Patent application number *(The Patent Office will fill in this part)*	15 JAN 1999 9900829.4
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	Patents ADP number *(if you know it)*	
	If the applicant is a corporate body, give the country/state of its incorporation	FINLAND 7406747001
4.	Title of the invention	[illegible] INTERFACE [illegible]
5.	Name of your agent *(if you have one)* "Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	NOKIA IPR DEPARTMENT NOKIA HOUSE SUMMIT AVENUE SOUTHWOOD FARNBOROUGH HAMPSHIRE GU14 ONZ UK
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		Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number			

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8.	Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:* *a) any applicant named in part 3 is not an inventor, or* *b) there is an inventor who is not named as an applicant, or* *c) any named applicant is a corporate body.* *See note (d))*	YES

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Description	~~15~~ 9
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11. I/We request the grant of a patent on the basis of this application.

Signature Paul Higgin Date 15/1/99

12. Name and daytime telephone number of person to contact in the United Kingdom: MR PAUL HIGGIN 01252 865283

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Interface

This document describes a proposal for a standard low-pin count RF/BB interface for Bluetooth.

Contents

1 Introduction

The purpose of this document is the specification of a standardized vendor and platform independent interface between the radio part (RF) and the baseband (BB) part of a Bluetooth (BT) system.

Important aspects of the Bluetooth system are described in co-pending UK patent application number GB9820859.8. The contents of these documents are hereby incorporated by reference, in particular, those parts relating to the implementation of the Bluetooth Low Power Radio Frequency System.

The benefit of a standardized interface is the interoperability of different RF and BB parts without HW changes. The low pin-count is particularly beneficial if the BB part is being integrated into another digital system e.g. a computer or phone chipset.

2 Interface Signals

The transfer of data and control information between the BB part and the RF part of a BT system is achieved using 2 three-wire interfaces (RFBus and Dbus) and an additional control signal SleepX.

The DBus is used to exchange general control data. The RFBus is used to transfer the transmitted and received data. In addition, time critical tasks during RX and TX are also performed via this bus.

Signal	Name	Direction	Function
1	RFBus1	bidirectional	RFBus
2	RFBus2	bidirectional	RFBus
3	BBClk	RF -> BB	RFBus (13 MHz)
4	DbusDa	Bidirectional	Dbus data
5	DbusClk	BB -> RF	Dbus clock
6	DbusEnX	BB -> RF	Dbus enable
7	VIO		Supply of the interfaces, 1.8V
8	SleepX	BB -> RF	

VIO supplies the voltage which the interfaces (RFBus, DBus SleepX) will use to define the logic levels. In this way, the interface can be run at a range of voltages to suit the particular application. At least a range of 1.8V+-10% need to be supported for VIO.

The VIO line is also used to supply the control circuitry to ensure that the system is controllable in power down mode.

SleepX is a control signal from the BB part to the RF part. If SleepX==LOW, the RF part is in low power mode. Additionally, the internal control logic is forced into the "Control Mode" (see below) and thus performs a similar functionality as a usual reset signal. There is no activity permitted on the RFBus and the DBus if SleepX==LOW and the BBClk is switched off.

2.1.1 RFBUS

The serial RFBus consists of 3 lines, that is BBClk, RFBus1 and RFBus2.
The BBClk is a 13 MHz clock generated in the RF part. It is used for synchronizing the data transferred via the RFBus. If applicable, it also might be used for clocking the logic of the baseband part.
Dependent on the mode of the RFBus, different functionality and direction of the signals RFBus1 and RFBus2 are specified.

Mode	Mode description	Functionality of the RFBUS1	Functionality of the RFBUS2	Direction of RFBUS1	Direction of RFBUS2
1	Control Mode	<CLKON>	0	BB -> RF	BB -> RF
2	Transmit Mode	<TXDATA>	<PAON>	BB -> RF	BB -> RF
3	Receive Mode	<RXDATA>	<DCTRACK>	RF -> BB	BB -> RF

The mode of the RFBus is controlled by the BB part. The state transitions are controlled via the DBus.

The CONTROL MODE is a neutral mode that is entered if neither RX nor TX mode applies. It is entered using the DBus or when SleepX==LOW. Thus SleepX can be considered as a reset signal as well. However, configuration registers in the RF part should not be reset using SleepX. They are programmed to their default states using the DBus. In Control mode, the signals RFBus1 and RFBus2 are driven by the BB part. In CONTROL MODE the 13 MHz clock (BBCLK) can be switched on by assigning RFBUS1==HIGH even if SleepX==LOW. Thus the clock is running if (SleepX==HIGH or (Mode=="Control Mode" and RFBUS1==HIGH)).

In TRANSMIT MODE the direction of RFBus1 and RFBus2 is from BB part to the RF part. RFBus1 is used to supply the digital transmit data <TXDATA> from the BB part to the RF part. Logic levels are used. The pulse shaping is done completely in the RF part and shall not depend on the value of VIO. Synchonization logic in the RF part shall ensure an exact symbol period of 1µs even if the data transferred on RFBus1=<TXDATA> exhibits substantial jitter. The line RFBus2 is used to control the timing of powering up the PA output stage of the RF part with RFBus2=<PAON>=HIGH.

In RECEIVE MODE the direction of RFBus1 is from RF part to the BB part and the direction of RFBus2 is from the BB part to the RF part. RFBus1 is used to supply sliced receive data at an oversampling ratio of 13 from the RF part to the BB part while using BBClk for synchronization. This is shown in the figure below.

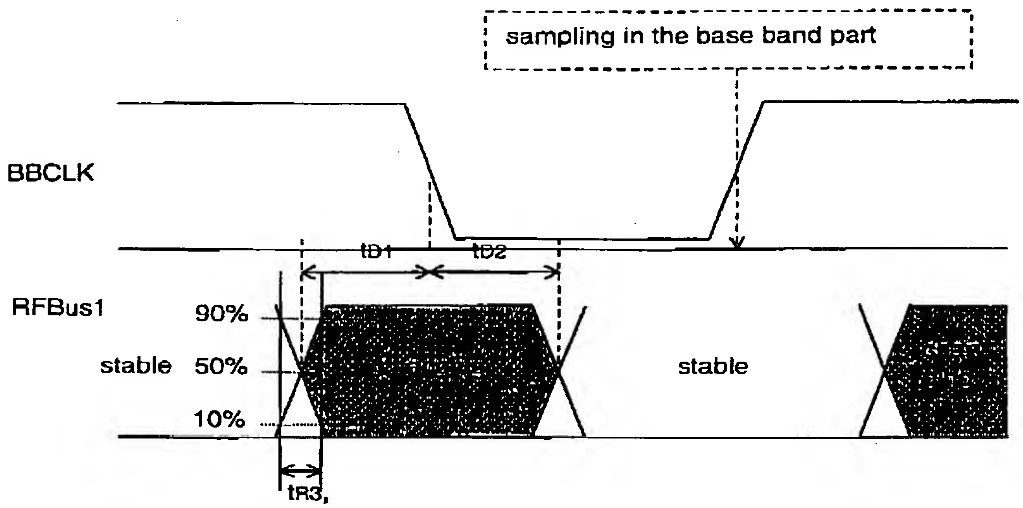

Figure 1: RFBUS1 output timing parameters

The receive data <RXDATA> are provided as sliced data to the BB part. This implies that the DC estimation functionality (carrier offset compensation) resides in the RF part. By means of the signal RFBus2 the BB part can control the DC estimation into 2 different states. During <DCTRACK>=LOW a method for fast acquisition of a DC estimate shall be used (reception of start of a packet). During <DCTRACK>=HIGH, slower DC estimators may be used for reception of the remaining packet.

2.1.2 Serial IO Data Bus (DBus)

The serial IO Data Bus (DBus) is a basic Clock, Data and Enable serial interface. The following sections outline the addressing, data length, access allocations and detailed protocol of the DBus.

The DBus is not dedicated purely to the interface between the RF part and the BB part. In the event that the BB functionality is integrated into another host system, the DBus may also be used to communicate with other devices with a maximum of 32 data bits. Therefore the complete 8 address bits plus one R/W bit have to be verified before latching data to permit bus sharing with devices that are used concurrently to the Bluetooth RF part. In this event the data word lengths can vary.

The DBusEnX line should be used to block the DBusDa and DBusClk line activity at the boundary of the RF part. In the event the RF part will have a dedicated enable line, this would allow isolation of the RF part from disturbances caused by activity on these lines due to other devices using the same DBus.

The DBus shall be operational at DBus clock speeds of up to 20 MHz. Note that the DBus clock is sufficient to clock the interface in the RF part. The 13 MHz clock is not used in the implementation of the DBus interface and it is not permissible to assume timing relations between the 13MHz clock and the DBus clock.

2.1.2.1 DBus Protocol

An access is always initiated by the DBus controlling device (e.g. the BT BB part). There are 3 device address bits and so a maximum of 8 devices can be addressed on the DBus. The device address of the BT RF part may either be programmable (using hard wired address pins) or fixed. If the BT RF part has a fixed address the address is 5 (101). Following the 3 device address bits there is a Read/Write bit which is then followed by 5 register address bits.

The preferred address allocation is:

Register Address Range	*Preferred Usage*
0-7	General programming, Mode control and RSSI reading (if applicable)
8-11	Control of optional 100mW PA (internal or external)
12-31	Reserved for future extensions

At the start of an access, the clock line (DBusClk) is reset to '0' and the Enable line (DBusEnX) is taken LOW half a clock cycle before the first positive clock edge to allow clean clock gating. At the first rising DBusClk edge the MSB of the address will be clocked into the RF part via the Data line (DBusDa).

The read and write access is arranged such that the addressed device will either read data or write data upon the rising edge of each clock pulse. This read and write protocol is described below. The Bluetooth RF part shall preferably be using 16 data bits after the address although the DBus protocol supports different lengths of the data words.

2.1.2.2 Dbus Write Access to the BT RF part

The controlling device will change the state of the data at the falling edge of each clock pulse. Following the 8 address bits, data bits are sent with the same timing as the address bits. Following the last data bit, the enable line is taken HIGH which indicates the arrival of the final data bit. The clock line then pulses one more pulse and is then held at '0' for a minimum of one cycle before a new access is started. The enable is therefore held HIGH for a minimum of two cycles.

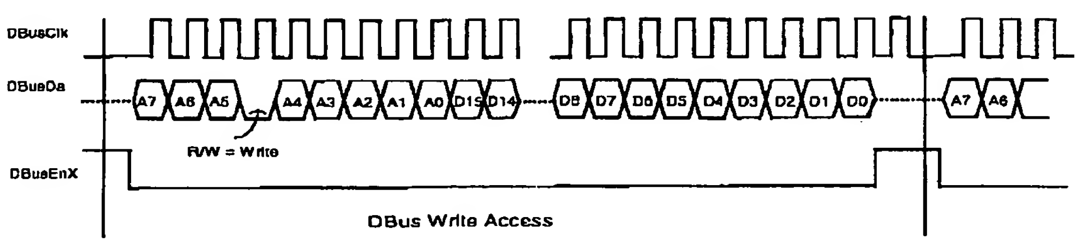

Figure 2 Write Access on Dbus (example with 16 bits of data)

2.1.2.3 Read Access from the BT RF part

During a read access the addressed device generates data on the DBus to be read by the controlling device. This time, following the 8 address bits there is a turn around bit which lasts for half a clock cycle and has the effect of realigning the DBus timing such that now the addressed device will load bits onto the DBus upon the rising edge of the DBusClk. The bits are therefore read upon falling edges. Following the last address bit, the DBusClk is again disabled for at least one clock cycle before the next access.

As with the write access, the data word length for the read access is not fixed. The preferred value is 16 data bits. The controlling side of the interface determines the number of data bits by the use of the enable line. Thus, the data word length must be fixed for a certain address.

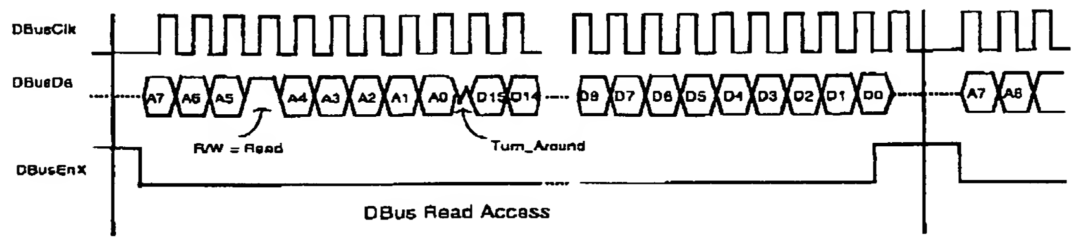

Figure 3 Read Access on Dbus (example with 16 bits of data)

2.1.2.4 DBus usage

All configuration data is send via the DBus as well as control words to switch between operational modes.

If data need to be read from the RF part (e.g. for RSSI measurements, etc.) the data is read digitally via the DBus rather than adding specific analog signals to the interface.

During power down (SleepX=LOW) the DBus shall not be used to ensure very low current consumption from VIO.

3 List of Acronyms and Abbreviations

BB	Base Band
RF	Radio Frequency
RX	Receive
TX	Transmit

One aspect of the present invention relates to a radio transceiver substantially as hereinbefore described with reference to the enclosed drawings and/or as shown in the drawings.

Another aspect of the present invention relates to an interface substantially as hereinbefore described with reference to the enclosed drawings and/or as shown in the drawings.

The present invention includes any novel feature or combination of features disclosed herein either explicitly or implicitly or any genaralisation thereof.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made to the foregoing description without departing from the scope of the invention.

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